

74AUP1T08-Q100

Low-power 2-input AND gate with voltage-level translator

Rev. 1 — 15 July 2021

Product data sheet

1. General description

The 74AUP1T08-Q100 provides the single 2-input AND function. This device ensures a very low static and dynamic power consumption across the entire V_{CC} range from 2.3 V to 3.6 V.

The 74AUP1T08-Q100 is designed for logic-level translation applications with input switching levels that accept 1.8 V low-voltage CMOS signals, while operating from either a single 2.5 V or 3.3 V supply voltage.

The wide supply voltage range ensures normal operation as battery voltage drops from 3.6 V to 2.3 V.

This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

Schmitt trigger inputs make the circuit tolerant to slower input rise and fall times across the entire V_{CC} range.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 2.3 V to 3.6 V
- High noise immunity
- ESD protection:
 - HBM JESD22-A114F Class 3A exceeds 5000 V
 - CDM JESD22-C101E exceeds 1000 V
- Low static power consumption; $I_{CC} = 1.5 \mu\text{A}$ (maximum)
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Inputs accept voltages up to 3.6 V
- Low noise overshoot and undershoot < 10 % of V_{CC}
- I_{OFF} circuitry provides partial power-down mode operation

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AUP1T08GW-Q100	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1

4. Marking

Table 2. Marking

Type number	Marking code ^[1]
74AUP1T08GW-Q100	5J

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

Fig. 1. Logic symbol

Fig. 2. IEC logic symbol

Fig. 3. Logic diagram

6. Pinning information

6.1. Pinning

Fig. 4. Pin configuration SOT353-1 (TSSOP5)

6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
B	1	data input
A	2	data input
GND	3	ground (0 V)
Y	4	data output
V _{CC}	5	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level.

Input		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
V_I	input voltage	[1]	-0.5	+4.6	V
I_{OK}	output clamping current	$V_O < 0$ V	-50	-	mA
V_O	output voltage	Active mode and Power-down mode [1]	-0.5	+4.6	V
I_O	output current	$V_O = 0$ V to V_{CC}	-	±20	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C [2]	-	250	mW

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT353-1 (TSSOP5) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		2.3	3.6	V
V_I	input voltage		0	3.6	V
V_O	output voltage	Active mode	0	V_{CC}	V
		Power-down mode; $V_{CC} = 0$ V	0	3.6	V
T_{amb}	ambient temperature		-40	+125	°C

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V _{T+}	positive-going threshold voltage	V _{CC} = 2.3 V to 2.7 V	0.60	-	1.10	V
		V _{CC} = 3.0 V to 3.6 V	0.75	-	1.16	V
V _{T-}	negative-going threshold voltage	V _{CC} = 2.3 V to 2.7 V	0.35	-	0.60	V
		V _{CC} = 3.0 V to 3.6 V	0.50	-	0.85	V
V _H	hysteresis voltage	(V _H = V _{T+} - V _{T-})				
		V _{CC} = 2.3 V to 2.7 V	0.23	-	0.60	V
		V _{CC} = 3.0 V to 3.6 V	0.25	-	0.56	V
V _{OH}	HIGH-level output voltage	V _I = V _{T+} or V _{T-}				
		I _O = -20 µA; V _{CC} = 2.3 V to 3.6 V	V _{CC} - 0.1	-	-	V
		I _O = -2.3 mA; V _{CC} = 2.3 V	2.05	-	-	V
		I _O = -3.1 mA; V _{CC} = 2.3 V	1.9	-	-	V
		I _O = -2.7 mA; V _{CC} = 3.0 V	2.72	-	-	V
		I _O = -4.0 mA; V _{CC} = 3.0 V	2.6	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{T+} or V _{T-}				
		I _O = 20 µA; V _{CC} = 2.3 V to 3.6 V	-	-	0.10	V
		I _O = 2.3 mA; V _{CC} = 2.3 V	-	-	0.31	V
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.44	V
		I _O = 2.7 mA; V _{CC} = 3.0 V	-	-	0.31	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.44	V
I _I	input leakage current	V _I = GND to 3.6 V; V _{CC} = 0 V to 3.6 V	-	-	±0.1	µA
I _{OFF}	power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V	-	-	±0.1	µA
ΔI _{OFF}	additional power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V to 0.2 V	-	-	±0.1	µA
I _{CC}	supply current	V _I = GND or V _{CC} ; I _O = 0 A; V _{CC} = 2.3 V to 3.6 V	-	-	1.2	µA
C _I	input capacitance	V _{CC} = 0 V to 3.6 V; V _I = GND or V _{CC}	-	0.8	-	pF
C _O	output capacitance	V _O = GND; V _{CC} = 0 V	-	1.7	-	pF

Low-power 2-input AND gate with voltage-level translator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +85 °C						
V _{T+}	positive-going threshold voltage	V _{CC} = 2.3 V to 2.7 V	0.60	-	1.10	V
		V _{CC} = 3.0 V to 3.6 V	0.75	-	1.19	V
V _{T-}	negative-going threshold voltage	V _{CC} = 2.3 V to 2.7 V	0.35	-	0.60	V
		V _{CC} = 3.0 V to 3.6 V	0.50	-	0.85	V
V _H	hysteresis voltage	(V _H = V _{T+} - V _{T-})				
		V _{CC} = 2.3 V to 2.7 V	0.10	-	0.60	V
		V _{CC} = 3.0 V to 3.6 V	0.15	-	0.56	V
V _{OH}	HIGH-level output voltage	V _I = V _{T+} or V _{T-}				
		I _O = -20 µA; V _{CC} = 2.3 V to 3.6 V	V _{CC} - 0.1	-	-	V
		I _O = -2.3 mA; V _{CC} = 2.3 V	1.97	-	-	V
		I _O = -3.1 mA; V _{CC} = 2.3 V	1.85	-	-	V
		I _O = -2.7 mA; V _{CC} = 3.0 V	2.67	-	-	V
		I _O = -4.0 mA; V _{CC} = 3.0 V	2.55	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{T+} or V _{T-}				
		I _O = 20 µA; V _{CC} = 2.3 V to 3.6 V	-	-	0.1	V
		I _O = 2.3 mA; V _{CC} = 2.3 V	-	-	0.33	V
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.45	V
		I _O = 2.7 mA; V _{CC} = 3.0 V	-	-	0.33	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.45	V
I _I	input leakage current	V _I = GND to 3.6 V; V _{CC} = 0 V to 3.6 V	-	-	±0.5	µA
I _{OFF}	power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V	-	-	±0.5	µA
ΔI _{OFF}	additional power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V to 0.2 V	-	-	±0.5	µA
I _{CC}	supply current	V _I = GND or V _{CC} ; I _O = 0 A; V _{CC} = 2.3 V to 3.6 V	-	-	1.5	µA
ΔI _{CC}	additional supply current	V _{CC} = 2.3 V to 2.7 V; I _O = 0 A [1]	-	-	0.6	µA
		V _{CC} = 3.0 V to 3.6 V; I _O = 0 A [2]	-	-	10	µA

Low-power 2-input AND gate with voltage-level translator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +125 °C						
V _{T+}	positive-going threshold voltage	V _{CC} = 2.3 V to 2.7 V	0.60	-	1.10	V
		V _{CC} = 3.0 V to 3.6 V	0.75	-	1.19	V
V _{T-}	negative-going threshold voltage	V _{CC} = 2.3 V to 2.7 V	0.33	-	0.64	V
		V _{CC} = 3.0 V to 3.6 V	0.46	-	0.85	V
V _H	hysteresis voltage	(V _H = V _{T+} - V _{T-})				
		V _{CC} = 2.3 V to 2.7 V	0.10	-	0.60	V
		V _{CC} = 3.0 V to 3.6 V	0.15	-	0.56	V
V _{OH}	HIGH-level output voltage	V _I = V _{T+} or V _{T-}				
		I _O = -20 µA; V _{CC} = 2.3 V to 3.6 V	V _{CC} - 0.11	-	-	V
		I _O = -2.3 mA; V _{CC} = 2.3 V	1.77	-	-	V
		I _O = -3.1 mA; V _{CC} = 2.3 V	1.67	-	-	V
		I _O = -2.7 mA; V _{CC} = 3.0 V	2.40	-	-	V
		I _O = -4.0 mA; V _{CC} = 3.0 V	2.30	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{T+} or V _{T-}				
		I _O = 20 µA; V _{CC} = 2.3 V to 3.6 V	-	-	0.11	V
		I _O = 2.3 mA; V _{CC} = 2.3 V	-	-	0.36	V
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.50	V
		I _O = 2.7 mA; V _{CC} = 3.0 V	-	-	0.36	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.50	V
I _I	input leakage current	V _I = GND to 3.6 V; V _{CC} = 0 V to 3.6 V	-	-	±0.75	µA
I _{OFF}	power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V	-	-	±0.75	µA
ΔI _{OFF}	additional power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V to 0.2 V	-	-	±0.75	µA
I _{CC}	supply current	V _I = GND or V _{CC} ; I _O = 0 A; V _{CC} = 2.3 V to 3.6 V	-	-	3.5	µA
ΔI _{CC}	additional supply current	V _{CC} = 2.3 V to 2.7 V; I _O = 0 A [1]	-	-	1.8	µA
		V _{CC} = 3.0 V to 3.6 V; I _O = 0 A [2]	-	-	18	µA

[1] One input at 0.3 V or 1.1 V, other input at V_{CC} or GND.

[2] One input at 0.45 V or 1.2 V, other input at V_{CC} or GND.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 6.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
V _{CC} = 2.3 V to 2.7 V; V _I = 1.65 V to 1.95 V										
t _{pd}	propagation delay	A, B to Y; see Fig. 5 [2]								
		C _L = 5 pF	2.0	3.3	5.2	0.5	6.8	0.5	7.5	ns
		C _L = 10 pF	2.3	3.9	6.0	1.0	7.9	1.0	8.7	ns
		C _L = 15 pF	2.7	4.4	6.6	1.0	8.7	1.0	9.6	ns
		C _L = 30 pF	3.5	5.5	8.1	1.5	10.8	1.5	11.9	ns
V _{CC} = 2.3 V to 2.7 V; V _I = 2.3 V to 2.7 V										
t _{pd}	propagation delay	A, B to Y; see Fig. 5 [2]								
		C _L = 5 pF	1.6	3.2	5.2	0.5	6.0	0.5	6.6	ns
		C _L = 10 pF	1.9	3.8	6.0	1.0	7.1	1.0	7.9	ns
		C _L = 15 pF	2.3	4.2	6.6	1.0	7.9	1.0	8.7	ns
		C _L = 30 pF	3.1	5.4	8.1	1.5	10.0	1.5	11.0	ns
V _{CC} = 2.3 V to 2.7 V; V _I = 3.0 V to 3.6 V										
t _{pd}	propagation delay	A, B to Y; see Fig. 5 [2]								
		C _L = 5 pF	1.2	2.9	4.7	0.5	5.5	0.5	6.1	ns
		C _L = 10 pF	1.6	3.5	5.4	1.0	6.5	1.0	7.2	ns
		C _L = 15 pF	1.9	4.0	6.1	1.0	7.4	1.0	8.2	ns
		C _L = 30 pF	2.7	5.1	7.5	1.5	9.5	1.5	10.5	ns
V _{CC} = 3.0 V to 3.6 V; V _I = 1.65 V to 1.95 V										
t _{pd}	propagation delay	A, B to Y; see Fig. 5 [2]								
		C _L = 5 pF	1.8	2.7	3.8	0.5	8.0	0.5	8.8	ns
		C _L = 10 pF	2.3	3.3	4.5	1.0	8.5	1.0	9.4	ns
		C _L = 15 pF	2.6	3.8	5.0	1.0	9.1	1.0	10.1	ns
		C _L = 30 pF	3.4	4.9	6.5	1.5	9.8	1.5	10.8	ns
V _{CC} = 3.0 V to 3.6 V; V _I = 2.3 V to 2.7 V										
t _{pd}	propagation delay	A, B to Y; see Fig. 5 [2]								
		C _L = 5 pF	1.5	2.6	4.0	0.5	5.3	0.5	5.9	ns
		C _L = 10 pF	1.9	3.2	4.8	1.0	6.1	1.0	6.8	ns
		C _L = 15 pF	2.1	3.7	5.4	1.0	6.8	1.0	7.5	ns
		C _L = 30 pF	2.9	4.8	6.9	1.5	8.5	1.5	9.4	ns
V _{CC} = 3.0 V to 3.6 V; V _I = 3.0 V to 3.6 V										
t _{pd}	propagation delay	A, B to Y; see Fig. 5 [2]								
		C _L = 5 pF	1.1	2.6	4.1	0.5	4.7	0.5	5.2	ns
		C _L = 10 pF	1.5	3.2	4.8	1.0	5.7	1.0	6.3	ns
		C _L = 15 pF	1.8	3.6	5.5	1.0	6.2	1.0	6.9	ns
		C _L = 30 pF	2.5	4.8	7.0	1.5	7.8	1.5	8.6	ns

Low-power 2-input AND gate with voltage-level translator

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
T _{amb} = 25 °C										
C _{PD}	power dissipation capacitance	f _i = 1 MHz; V _I = GND to V _{CC} [3]								
		V _{CC} = 2.3 V to 2.7 V	-	4	-	-	-	-	-	pF
		V _{CC} = 3.0 V to 3.6 V	-	5	-	-	-	-	-	pF

- [1] All typical values are measured at nominal V_{CC}.
- [2] t_{pd} is the same as t_{PLH} and t_{PHL}.
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
Σ(C_L × V_{CC}² × f_o) = sum of the outputs.

11.1. Waveform and test circuit

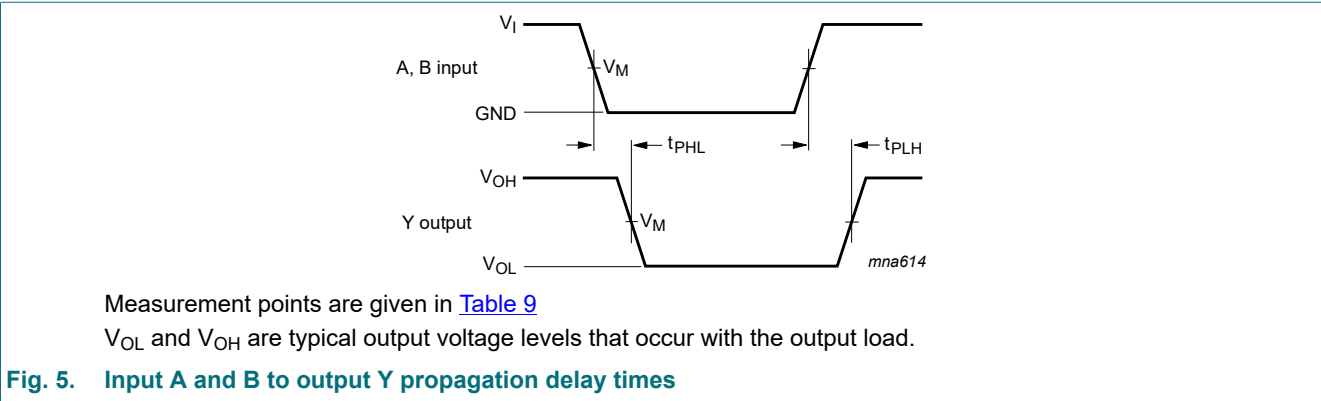
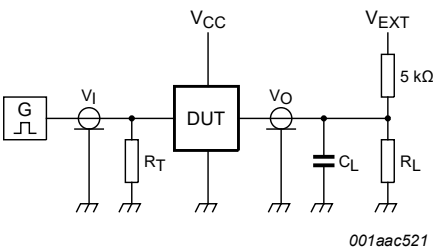


Table 9. Measurement points

Supply voltage	Output	Input		
V _{CC}	V _M	V _M	V _I	t _r = t _f
2.3 V to 3.6 V	0.5 × V _{CC}	0.5 × V _I	1.65 V to 3.6 V	≤ 3.0 ns



Test data is given in [Table 10](#).
Definitions for test circuit:
 R_L = Load resistance.
 C_L = Load capacitance including jig and probe capacitance.
 R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.
 V_{EXT} = External voltage for measuring switching times.

Fig. 6. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Load		V_{EXT}		
V_{CC}	C_L	R_L [1]	t_{PLH} , t_{PHL}	t_{PZH} , t_{PHZ}	t_{PZL} , t_{PLZ}
2.3 V to 3.6 V	5 pF, 10 pF, 15 pF and 30 pF	5 kΩ or 1 MΩ	open	GND	$2 \times V_{CC}$

[1] For measuring enable and disable times $R_L = 5\text{ k}\Omega$.
For measuring propagation delays, setup and hold times and pulse width $R_L = 1\text{ M}\Omega$.

12. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm

SOT353-1

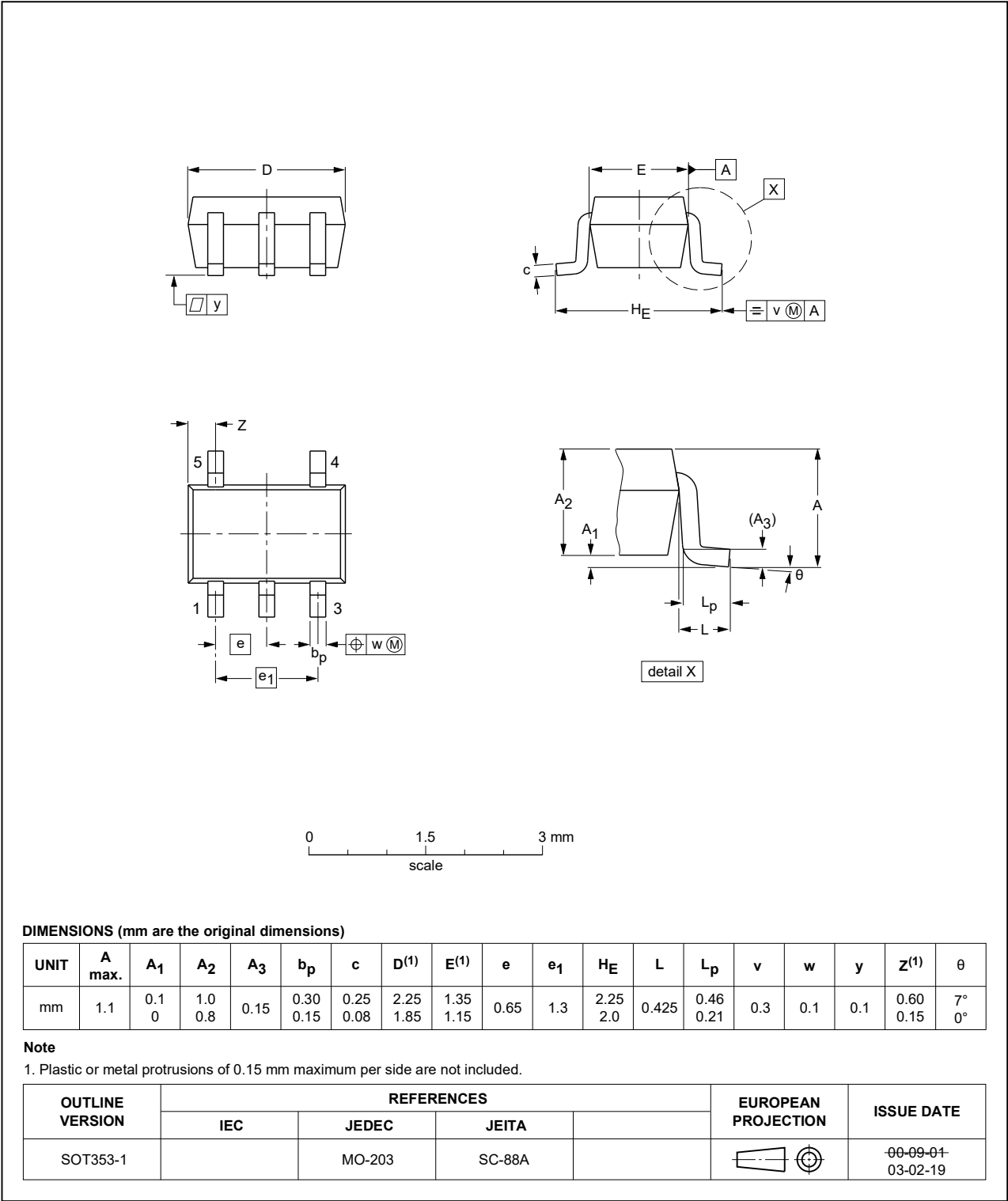


Fig. 7. Package outline SOT353-1 (TSSOP5)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AUP1T08_Q100 v.1	20210715	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
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Contents

1. General description	1
2. Features and benefits	1
3. Ordering information	1
4. Marking	2
5. Functional diagram	2
6. Pinning information	2
6.1. Pinning	2
6.2. Pin description	2
7. Functional description	3
8. Limiting values	3
9. Recommended operating conditions	3
10. Static characteristics	4
11. Dynamic characteristics	7
11.1. Waveform and test circuit	8
12. Package outline	10
13. Abbreviations	11
14. Revision history	11
15. Legal information	12

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